Mentor Graphics announce New formal-based technologies in the Questa Verification Platform

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Mentor Graphics announce new formal-based technologies in the Questa Verification Platform that provide mainstream users with the ability to more easily perform exhaustive formal verification analysis. The new Questa AutoCheck technology delivers fully automated formal checking analysis, while the Questa CoverCheck tool provides 100% code coverage closure. The Questa Verification Platform now also offers expanded clock-domain crossing capabilities.

Formal verification offers exhaustive functional analysis of all possible design behaviours without the need to specify the test stimulus, enabling verification early in the design cycle, before creation of a simulation testbench. However, in the past, the promise of formal verification was only realized by verification teams with formal analysis experts that had to expend a high amount of effort to achieve results. The Questa platform changes all that by delivering a wide spectrum of formal applications that range from fully automatic formal checking with AutoCheck, a powerful, push-button technology that everyone can easily use, to property checking with custom coded assertions for advanced users. The Questa platform now offers a broad arsenal of verification solutions that seamlessly blend simulation and formal-based technologies with common compilation and user interface features as well as the Unified Coverage Database.

Questa CoverCheck Enables 100% Code Coverage Closure The Questa CoverCheck technology accelerates the process of code coverage closure. Code coverage closure typically involves many engineering weeks of effort to manually review code coverage holes to determine if they can be safely ignored and if not, to generate hand-crafted simulation tests to cover them. Questa CoverCheck makes it easy for non-expert users to leverage formal methods to complete this process by automatically identifying the set of reachable and unreachable coverage bins. Consequently, it significantly reduces the time required for code coverage sign-off, bringing predictability to the schedule. CoverCheck also ensures higher design quality by preventing bugs from slipping through the verification process due to mistakenly ignored code coverage bins.

Questa Formal with AutoCheck for Mainstream Users AutoCheck analyses RTL designs and automatically synthesizes assertions that are then processed by powerful formal engines to check for correct sequential design behaviour. Using AutoCheck, designs are easily verified to be free from common functional errors without the need to write a testbench or assertions. In addition, performance improvements based on breakthrough formal engines and formal model optimizations deliver improved quality of results and a significant decrease in compute resource consumption. This release also delivers Questa Formal Multi-Core, a new capability that enables multi-core and multi-computer distribution of formal jobs, further improving the throughput of formal analysis and optimizing the use of compute farm resources.

One of the challenges to achieving a high degree of verification quality is the wide spectrum of functional problems that must be accounted for, ranging from common RTL coding errors to obscure corner case bugs, said Dr. Byeong E. Min, master of System LSI infrastructure design center, Device Solutions, Samsung Electronics. We are pleased with the enhanced verification productivity and design quality that we have achieved by deploying formal-based technologies in the Questa platform, which address some of these problem areas that are not well covered by traditional methods.

Questa CDC for High Performance Analysis and Unlimited Design Sizes Questa CDC is used extensively by leading semiconductor design teams and it sets the bar for capacity, ease of use and quality of results. This release delivers additional performance gains, boosting the capacity of Questa CDC to match the complexity of today’s SoC designs. Questa CDC also supports unlimited design sizes through hierarchical CDC analysis. It automatically generates highly accurate, block-level CDC interface logic models that enable chip-level CDC verification with full debug visibility.

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On an industry-wide basis, we are seeing increased demand for high-performance, easy-to-use formal methods in order to reduce the overall time to verification in terms of human and technical resources, said John Lenyo, vice president and general manager of the Design Verification Technology division of Mentor Graphics. The new formal-based capabilities of the Questa platform make it very attractive in terms of both state-of-the-art performance and capacity advances, as well as practical in terms of automation, to incorporate the power of formal technology into existing verification flows.

The new release of Questa CoverCheck, Questa CDC and Questa Formal is available immediately.